IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

VIASAT, INC., **Plaintiff,** **vs.** **WESTERN DIGITAL CORPORATION and WESTERN DIGITAL TECHNOLOGIES, INC.,** **Defendants.**	**Case No.: 6:21-cv-01230-ADA** **JURY TRIAL DEMANDED**
VIASAT, INC., **Plaintiff,** **vs.** **KIOXIA CORPORATION and KIOXIA AMERICA, INC.,** **Defendants.**	**Case No.: 6:21-cv-01231-ADA** **JURY TRIAL DEMANDED**

DECLARATION OF MEG E. FASULO IN SUPPORT OF PLAINTIFF VIASAT, INC.'S RESPONSE TO DEFENDANTS' OPENING CLAIM CONSTRUCTION BRIEF

I, Meg E. Fasulo, declare as follows:

1. I am an attorney with the law firm Bartlit Beck LLP and counsel for Plaintiff Viasat, Inc. I have been admitted pro hac vice in Case Nos. 6:21-cv-01230-ADA and 6:21-cv-01231-ADA.

2. I provide this declaration in support of Viasat, Inc.'s Response to Defendants' Opening Claim Construction Brief. I submit this declaration based upon my personal knowledge

and my investigation of the facts below. If called upon to testify, I could and would testify competently to these facts.

3. Attached as Exhibit 1 is a true and correct copy of the Declaration of Professor Nader Bagherzadeh, Ph.D. regarding Claim Construction, dated August 23, 2022.

4. Attached as Exhibit 2 is a true and correct copy of U.S. Patent No. 8,615,700, dated December 24, 2013.

5. Attached as Exhibit 3 is a true and correct copy of excerpts from Kioxia Corporation and Kioxia America, Inc.'s Petition for *Inter Partes* Review of Claims 1-4, 8, 10-19, and 23-25 of U.S. Patent No. 8,615,700, No. IPR2022-01067, dated May 31, 2022.

6. Attached as Exhibit 4 is a true and correct copy of Artur Jorge Alves Antunes, VERILOG IMPLEMENTATION OF A FORWARD ERROR CORRECTING REED SOLOMON ENCODER AND DECODER (2017).

7. Attached as Exhibit 5 is a true and correct copy of Hanho Lee, *High-Speed VLSI Architecture for Parallel Reed-Solomon Decoder*, 11(2) IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS 288-294 (2003).

8. Attached as Exhibit 6 is a true and correct copy of Bei Huang et al., *An Area Efficient Multi-Mode Architecture for Reed-Solomon Decoder*, 2009 IEEE 8TH INTERNATIONAL CONFERENCE ON ASIC 505-508 (2009).

9. Attached as Exhibit 7 is a true and correct copy of Bainan Chen et al., *Error Correction for Multi-Level NAND Flash Memory Using Reed-Solomon Codes*, 2008 IEEE WORKSHOP ON SIGNAL PROCESSING SYSTEMS 94-99 (2008).

10. Attached as Exhibit 8 is a true and correct copy of Maryam Ashouei et al., *Improving SNR for DSM Linear Systems Using Probabilistic Error Correction and State*

Restoration: A Comparative Study, ELEVENTH IEEE EUROPEAN TEST SYMPOSIUM (ETS'06) 35-42 (2006).

11. Attached as Exhibit 9 is a true and correct copy of Micron Technology, Inc., *ECC Module for Xilinx Spartan-3*, dated May 1, 2007.

12. Attached as Exhibit 10 is a true and correct copy of excerpts from Western Digital Technologies, Inc.'s Petition for *Inter Partes* Review, No. IPR2022-01126, dated June 10, 2022.

13. Attached as Exhibit 11 is a true and correct copy of excerpts from Western Digital Technologies, Inc.'s Petition for *Inter Partes* Review, No. IPR2022-01171, dated June 22, 2022

14. Attached as Exhibit 12 is a true and correct copy of S. A. Abbasi, *FPGA based realization of a reduced complexity high speed decoder for error correction*, 10TH IEEE INTERNATIONAL CONFERENCE ON ELECTRONICS, CIRCUITS AND SYSTEMS 1002-1005 (2003).

15. Attached as Exhibit 13 is a true and correct copy of excerpts from Charles H. Roth, Jr. & Larry L. Kinney, FUNDAMENTALS OF LOGIC DESIGN (6th ed. 2010).

16. Attached as Exhibit 14 is a true and correct copy of U.S. Patent No. 6,751,766, dated June 15, 2004.

17. Attached as Exhibit 15 is a true and correct copy of U.S. Patent No. 8,966,347, dated February 24, 2015.

18. Attached as Exhibit 16 is a true and correct copy of Cadence Design Systems, Inc. Design IP Datasheet, *Controller IP for NAND Flash* (2019).

19. Attached as Exhibit 17 is a true and correct copy of Frank Vahid, *Chapter 2: Combinational Logic Design (Slides)*, DIGITAL DESIGN (1st ed. 2007).

20. Attached as Exhibit 18 is a true and correct copy of Frank Vahid, *Chapter 9: Hardware Description Languages (Slides)*, DIGITAL DESIGN (1st ed. 2007).

21. Attached as Exhibit 19 is a true and correct copy of excerpts from Exhibit 1002 to Kioxia Corporation and Kioxia America, Inc.'s Petition for *Inter Partes* Review (No. IPR2022-01067) entitled *Expert Declaration of Richard Koralek Ph.D. for Inter Partes Review of U.S. Patent No. 8,615,700*, dated May 30, 2022.

22. Attached as Exhibit 20 is a true and correct copy of Song-Chul Jang et al., *Design of Parallel BCH Decoder for MLC Memory*, 2008 INTERNATIONAL SOC DESIGN CONFERENCE III-46-III-47 (2008).

23. Attached as Exhibit 21 is a true and correct copy of Bainan Chen et al., *Error Correction for Multi-Level NAND Flash Memory Using Reed-Solomon Codes* (unpublished PowerPoint, Case Western Reserve University) (2008).

24. Attached as Exhibit 22 is a true and correct copy of Sangeeta Singh & S. Sujana, *ASIC Implementation of Reed Solomon Codec for Burst Error Detection and Correction*, 2(4) INT'L J. ENG. RES. 1828-1832 (2013).

25. Attached as Exhibit 23 is a true and correct copy of excerpts from Rino Micheloni et al., ERROR CORRECTION CODES FOR NON-VOLATILE MEMORIES (2010).

I declare under penalty of perjury that the foregoing is true and correct.

Executed on August 23, 2022 in Denver, Colorado.

/s/ Meg E. Fasulo
Meg E. Fasulo